13 NEGATIVE-RESISTANCE SWITCHING CIRCUITS

We consider, in this chapter, circuit applications of the negative-resistance devices introduced in Chap. 12. Certain generalized circuit properties of negative-resistance devices are described first. We then establish the principles which allow us to determine the mode of operation of the circuit: bistable, monostable, or astable. Finally, these general principles are applied to account for the particular behavior of circuits employing the negative-resistance devices described in the preceding chapter.

13-1 THE NEGATIVE-RESISTANCE CHARACTERISTIC[1]

The devices of interest to us display, between a selected set of terminals, a volt-ampere characteristic such as is represented, in somewhat generalized form, in either Fig. 13-1*a* or *b*. In Fig. 13-1*a*, between 0 and A and to the right of the point B the device has a positive incremental resistance, whereas between A and B the incremental resistance is negative since, as may be noted, an *increase* in voltage causes a *decrease* in current. Similarly, in Fig. 13-1*b*, the portion of the characteristic between A and B displays a negative incremental resistance. For the sake of simplicity, and with no loss in generality of principle, we have made the characteristics piecewise linear and have arranged that they pass through the origin. This feature is in no way essential to the present discussion, although actually we see in Chap. 12 that all characteristics except that of the unijunction transistor do indeed pass through the origin. In addition, the characteristics have the general form shown in Fig. 13-1 without being piecewise linear.

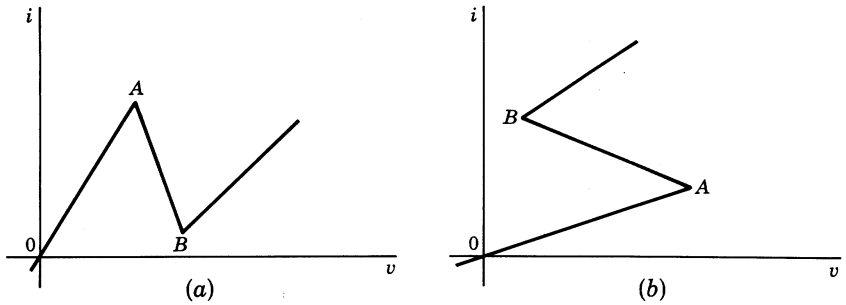

Fig. 13-1 (*a*) A voltage-controllable negative-resistance characteristic; (*b*) a current-controllable negative-resistance characteristic.

We observe in Fig. 13-1*a* that associated with each voltage there is a unique current, but the plot does not everywhere associate a unique voltage with each current. In the plot of Fig. 13-1*b* the inverse applies. To distinguish the one from the other we call the characteristic in Fig. 13-1*a* *voltage-controllable* and in Fig. 13-1*b* *current-controllable*. The tunnel diode falls into the voltage-controllable class, whereas all of the other devices discussed in the preceding chapter (the UJT, *p-n-p-n* diode, SCS, thyristor, and avalanche transistor) have a current-controllable characteristic.

13-2 BASIC CIRCUIT PRINCIPLES

We shall show that a device with a region of negative incremental resistance may be used to construct a switching circuit. The two classes of negative-resistance (NR) devices must be considered separately since the basic circuit of one type is essentially the dual of the other. We shall consider the current-controlled NR device first. The basic circuit is indicated in Fig. 13-2*a*, where a source of voltage V and a resistor R are shown connected to an NR device with the volt-ampere characteristic of Fig. 13-2*b*. Shunted across the NR device is a capacitor C, which may represent stray capacitance or capacitance deliberately introduced.

The voltage v across the device is the supply voltage V less the drop across R. If i_R is the current through R, then

$$v = V - i_R R \tag{13-1}$$

The device current is i and the capacitor current is i_C. We are interested in the steady state corresponding to a particular value of supply voltage, say $V = V_1$. When the currents and voltages in the circuit stop changing, $i_C = 0$ and $i_R = i$. Hence, on the same set of coordinate axes on which is plotted the device characteristic we have drawn the load line corresponding to Eq. (13-1) with $i_R = i$. This line is plotted in Fig. 13-2*b* as the solid line

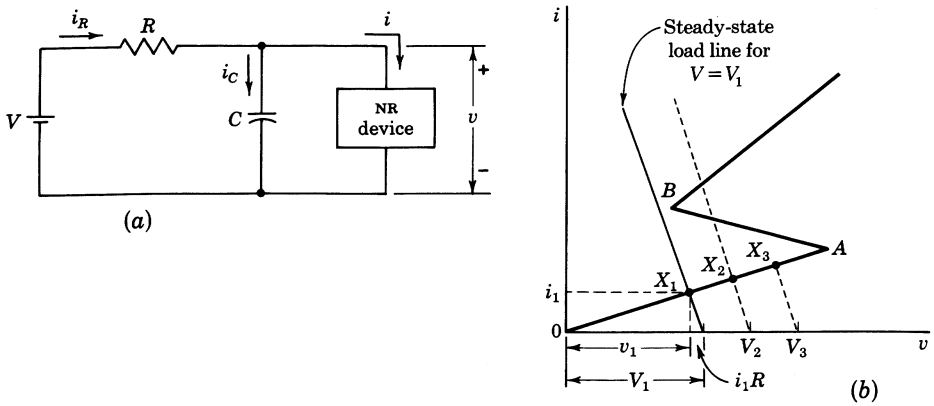

Fig. 13-2 (a) A circuit involving a current-controllable negative-resistance (NR) device; (b) the load line corresponding to supply voltage $V = V_1$ and resistance R is superimposed on the NR device characteristic in a manner to yield one stable equilibrium point at X_1.

passing through the point $v = V_1$, $i = 0$, and having a slope $-1/R$. Under steady-state conditions, the point of operation of the circuit must lie on the device characteristic and simultaneously on the load line. Hence, corresponding to the particular supply V_1 the steady-state current and voltage are i_1 and v_1, respectively, corresponding to point of intersection X_1 of the load line and the device characteristic.

Now let there be added to the supply a step of voltage which makes the new supply voltage $V = V_2$. The new load line is shown dashed, and the new steady-state operating point will be at X_2. A time will elapse before this new steady-state condition is reached, since the capacitor must change its voltage. The capacitor charges through an equivalent resistance which is equal to the parallel combination of R and the (positive) resistance of the NR device over the region OA. We shall now prove that in response to the change in supply voltage from V_1 to V_2 the operating point of the device moves from its original position at X_1 in the direction toward X_2. This result seems obvious enough at the present time, but in establishing the proof, we shall arrive at a result which will be quite useful in the following discussion. We have from Fig. 13-2*a* that

$$i_R = i_C + i = C\frac{dv}{dt} + i \tag{13-2}$$

Combining Eq. (13-2) with Eq. (13-1) we find that

$$RC\frac{dv}{dt} = V - (iR + v) \tag{13-3}$$

Now suppose that the NR device is operating at a particular point X_E where $i = i_E$ and $v = v_E$. Then $V_E = i_ER + v_E$ is the supply voltage which would make operation at i_E and v_E an equilibrium point. Suppose, however, that the supply voltage is not V_E but is instead V_S. Then Eq. (13-3) may be written

$$RC\frac{dv}{dt}\bigg|_{X_E} = V_S - V_E \tag{13-4}$$

Expressing Eq. (13-4) in words, we have the following theorem: *If the device is operating at X_E, which would be an equilibrium point if the supply voltage were V_E, but if in reality $V = V_S$, then dv/dt is positive if $V_S > V_E$. Alternatively, if $V_S < V_E$ then dv/dt is negative.* Applying this result to Fig. 13-2*b* we note that when the supply voltage is abruptly increased to V_2 ($= V_S$), then since $V_2 > V_1$ ($= V_E$), dv/dt is positive and the operating point moves to the right along the device characteristic in the direction of increasing v.

We may use Eq. (13-4) to prove that a point such as X_2 in Fig. 13-2*b*, corresponding to the intersection of the device characteristic with the load line passing through X_2, is a *stable* operating point. That is, if the circuit is perturbed in some manner so that the operating point is caused to depart from X_2, it will return to X_2. Such a perturbation might be caused by removing the capacitor, changing the voltage across it, and then replacing it in the circuit. Suppose that as the result of such a maneuver the operating point is established momentarily at $X = X_1$ in Fig. 13-2. Then Eq. (13-4) with $V_S = V_2$ and $V_E = V_1$ indicates $dv/dt\,|_{X_1} > 0$. Hence there will be an increase in v which will carry the operating point back to X_2. Similarly, if X were located to the right of X_2, say at $X = X_3$, then Eq. (13-4) would become, with X_E replaced by X_3, $V_E = V_3$, and $V_S = V_2$,

$$RC\frac{dv}{dt}\bigg|_{X_3} = V_2 - V_3 \tag{13-5}$$

Since $V_2 < V_3$, then $dv/dt < 0$ and v decreases so as to carry the operating point from X_3 back to X_2. We have thus verified that X_2 is a stable point regardless of whether a disturbance momentarily increases or decreases the voltage across the device.

We shall now apply the above principles to show that the basic circuit of Fig. 13-2*a* may be made to function in a monostable, bistable, or astable mode, depending upon the biasing method.

13-3 MONOSTABLE OPERATION

Consider the situation depicted in Fig. 13-3. The supply voltage is initially V_1, and the steady-state operating point is at X_1. A voltage step added to V increases the supply voltage to V_2, carrying the new load line beyond the critical point A, so that a new steady state will be established at X_2. The

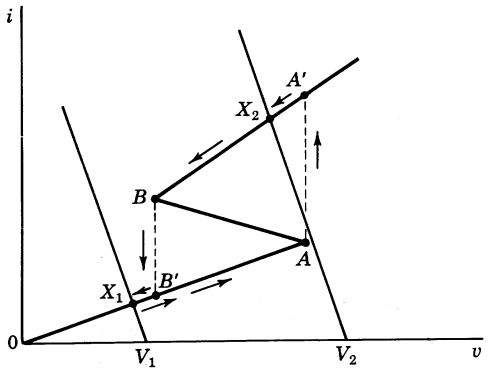

Fig. 13-3 Illustrating the abrupt transitions which occur when the load line moves beyond a critical point such as A or B.

operating point of the device must, of course, remain on the device characteristic as it moves toward X_2. Accordingly, the operating point initially moves to the point A. We may now apply the principle of Eq. (13-4) to establish that dv/dt is positive at A. Hence, the operating point cannot continue its approach toward X_2 by moving along AB, because along this path dv/dt would be negative. The only alternative is to have the operating point jump abruptly vertically from A to A'. By applying Eq. (13-4) at A' we find that dv/dt is negative. The operating point may therefore continue toward X_2 by moving toward the left along $A'B$. The device has, by taking this operating path, avoided behaving inconsistently with Eq. (13-4), but there now exists an anomalous situation in that the path has departed from the device characteristic. We may, however, take a philosophical attitude toward this matter and judge that if the transition from A to A' is completed in *zero time*, then actually the operating point has not really left its characteristic. Returning to the circuit of Fig. 13-2*a* we find no inconsistency in making the abrupt jump from A to A'. Specifically, the voltage has not changed instantaneously, as indeed it may not, because of the capacitor. The current has changed abruptly. There is nothing in this idealized circuit to restrain it from so doing.

With a physical NR device, we expect and observe, in a corresponding situation, a rapid but hardly instantaneous transition. First, realistic circuits and devices have all sorts of stray inductances and capacitances not contemplated in the discussion above. Second, a physical device has an NR region which does not really exist initially at all but is rather generated when a certain critical voltage or current is reached. To complete creating this region will ordinarily require a finite time interval. For example, in an avalanche transistor a negative resistance results from the cumulative generation of current carriers resulting from the disruption of atomic bonds. A finite time is required for this cumulative avalanche process to build up and for certain other redistributions required of the stored charge in the transistor. Thus when stray inductance or capacitance is reduced to a minimum the speed of the transition depends very greatly on the mechanism internal to the device by which the NR region is generated.

A discussion analogous to that given above leads to the conclusion that if, after X_2 has been attained, the supply voltage is returned to V_1, then the operating point will return to X_1. From X_2 the operating point will move relatively slowly to B, make an abrupt transition to B', and finally return to X_1. The complete path of the operating point is indicated by the arrows.

In order to induce this transition from the original stable low-current operating point X_1 to a temporary high-current state and back again, it is only necessary that the step of voltage have an amplitude adequate to carry the load line beyond A and last long enough to allow the operating point to reach the point A'. Thus the total transition to a quasi-stable state and back again may be induced by a pulse. Accordingly, we have just described the operation of a *monostable* generator of fast waveforms.

One-shot operation is also possible by establishing a quiescent voltage more positive than that at point A and then applying a negative pulse of large enough magnitude and long enough duration to carry the operating point to the left of B.

We have achieved triggering by superimposing a pulse on the supply voltage to carry the load line beyond a critical point A. In many physical devices (those with additional terminals other than the ones between which the negative-resistance characteristic appears) a triggering pulse applied to one of these extra terminals will achieve triggering by modifying the device characteristic. Thus instead of moving the load line to the right of point A, the triggering pulse may achieve triggering by moving the critical point to the left of X_1 while the load line remains stationary.

13-4 BISTABLE OPERATION

A bistable circuit is generated by selecting a supply voltage and load resistor that give rise to a load line which intersects the device characteristic in three places, X, Y, and Z, as in Fig. 13-4. If the circuit is initially at X, then a positive pulse added to the supply voltage will carry the operating point

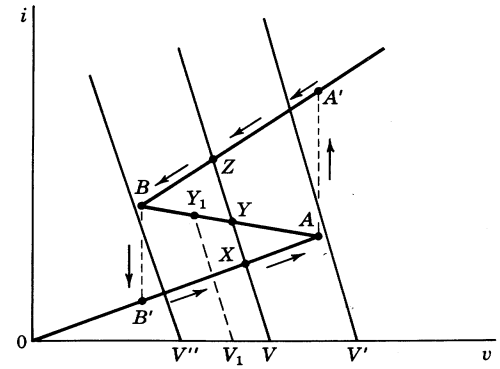

Fig. 13-4 The load line passing through V and intersecting the characteristic in three places allows bistable operation.

in the direction of the arrows to the stable operating point Z, where the circuit will remain permanently. Again the pulse must be adequate in amplitude to carry the load line beyond point A, as, for example, is the case with the load line passing through V'. Also, the pulse duration must be long enough to allow the operating point to reach A'. After the circuit is established at Z a negative pulse that carries the load line to the left, as is the case with the load line passing through V'', will return the circuit to X. Thus the circuit has two stable states and may be triggered from one state to the other by applying alternate positive and negative pulses.

The intersection point at Y on the negative-resistance portion of the characteristic is also a stable point, as may readily be verified. Consider, for example, that a momentary disturbance has shifted the operation to point Y_1. Then, since $V_1 < V$, Eq. (13-4) indicates that dv/dt is positive. Hence v increases and the operating point moves from Y_1 toward Y, thus confirming that Y is a stable point. Operation at Y, however, will ordinarily not be attained because in the triggering scheme we have described it is simply not accessible.

13-5 ASTABLE OPERATION

An astable waveform is generated by selecting a supply voltage and load resistor such that the load line intersects the characteristic at a single point X on the NR portion of the characteristic, as in Fig. 13-5. The important distinction between the present case and the situation which gave rise to the bistable circuit is that in the present case the equilibrium point at X is unstable. If a perturbation causes an initial departure of the operating point from X, the subsequent response of the circuit is to carry the operating point still farther from the equilibrium point. That such is the case in the present instance may be seen by an application of Eq. (13-4). Thus, suppose that with the equilibrium point at X a perturbation moves the operating point to X_1. Since now $V_1 > V$, we see, from Eq. (13-4), that dv/dt is correspondingly negative, and the operating point which momentarily was displaced to X_1

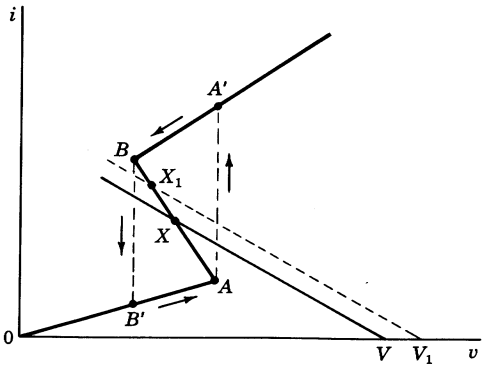

Fig. 13-5 Adjustment of the load line for astable operation.

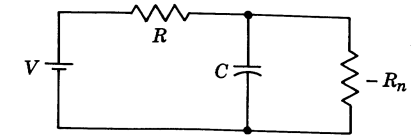

Fig. 13-6 Circuit equivalent to the network of Fig. 13-2a for small voltage excursions in the negative-resistance region.

moves still farther from X toward B. Similarly, if X_1 were below X, the operating point would move toward A.

We now take up a second way of establishing the instability of the equilibrium point at X. For this purpose consider the equivalent circuit of Fig. 13-6, where, since the NR device is operating in its NR region, we have replaced the device by a negative resistance of magnitude R_n. This configuration, with $V = 0$, is an equivalent circuit for the purpose of computing incremental changes from an initial equilibrium state. The circuit has a single time constant given by $R_\parallel C$, where $R_\parallel$ is the parallel combination of R and $-R_n$, that is,

$$R_\parallel = \frac{-R_n R}{R - R_n} \tag{13-6}$$

Now $R_\parallel$ is positive or negative as R_n is larger or smaller than R. If an equilibrium state is perturbed, the subsequent response will be of the form $\epsilon^{-t/R_\parallel C}$. If $R_n > R$, then $R_\parallel > 0$, and the circuit responds in accordance with a negative exponential back to its equilibrium state. The equilibrium state is then stable. If $R_n < R$, then $R_\parallel < 0$, and the response has the form of an exponential with a positive exponent. The operating point therefore moves farther away from its initial equilibrium state, picking up speed as it goes. We observe that in Fig. 13-5, $R_n < R$, which is consistent with our previous conclusion that the equilibrium state is unstable. We may also note that again, as expected, on the basis of our present manner of establishing stability, the state at Y in Fig. 13-4 is stable because $R_n > R$.

Returning now to Fig. 13-5 we observe that, starting from an initial state at X, a small disturbance will start the circuit toward either B or A, depending on the direction of the disturbance. Thereafter, the system will trace out the path $BB'AA'B$ in the direction of the arrows, with no need for continued external triggering. The circuit is astable and generates two abrupt current transitions per cycle.

We noted above that a current-controlled NR device would be stable even in its negative-resistance region provided that $R_n > R$. If we desire stability no matter what the value of R_n may be, we require that $R = 0$. For this reason a current-controlled NR device is often characterized as being "short-circuit stable." Similarly, we shall see later that a voltage-controlled device is "open-circuit stable."

Both of the arguments given above to prove that X is an unstable point depended upon the existence of a capacitance across the NR device. If, ideally, C could be reduced to zero, then stable operation at point X would be possible. In practice it turns out that if C is smaller than a certain "critical"

value, then a stable state at X is indeed obtained. This critical capacitance for most NR devices is of the order of some tens of picofarads, although its exact value is difficult to calculate. In order to do so it is necessary to include in Fig. 13-6 the inductance of the device along with wiring inductances and then solve for the minimum value of the capacitance that gives a positive real part to the roots of the equation determining the transient response (or, equivalently, to the poles of the network function). In summary, if the shunt capacitance across a current-controlled NR device is below some tens of picofarads, then a point on the NR portion of the characteristic is stable. However, for capacitances larger than critical it becomes unstable.

13-6 VOLTAGE-CONTROLLED NEGATIVE-RESISTANCE SWITCHING CIRCUITS

We consider now the voltage-controlled NR device whose characteristic appears again in Fig. 13-7*b*. The appropriate circuit for switching operation is now shown in Fig. 13-7*a*. Comparing Fig. 13-7*a* with Fig. 13-2*a* we note that the shunt capacitor has been replaced by a series inductor. Analogously to the current-controlled case, load lines passing through supply voltages V, V', and V'' are appropriate to astable, bistable, and monostable operation, respectively. Note that the monostable line intersects the device characteristic at one point along a positive-resistance portion. The bistable line has three points of intersection, two along positive-resistance branches and the third on the negative-resistance section. The astable line intersects the characteristic at one point along the negative-resistance segment.

The stability of an operating point may be investigated in one of two ways. First, from Fig. 13-7*a* we have

$$L\frac{di}{dt} = V - iR - v \tag{13-7}$$

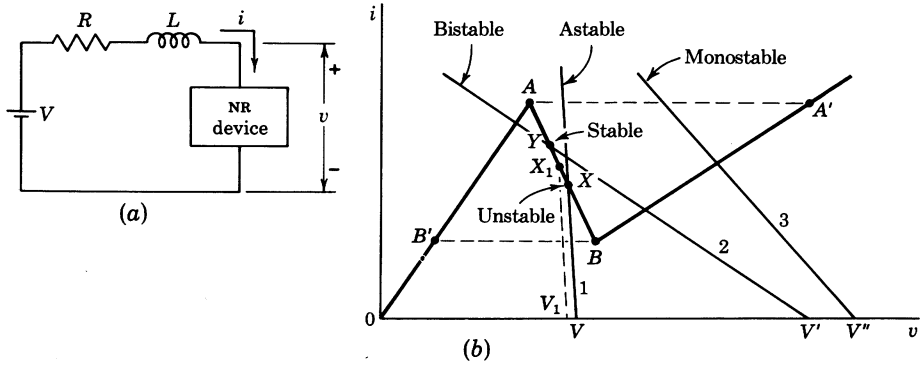

Fig. 13-7 (*a*) A circuit involving a voltage-controlled negative-resistance device; (*b*) characteristic and load lines for bistable, astable, and monostable operation.

If the operating point is momentarily at $X_E(i_E, v_E)$, where $i_E R + v_E = V_E$, and if the supply voltage is V_S, then this equation may be written

$$L\frac{di}{dt}\bigg|_{X_E} = V_S - V_E \tag{13-8}$$

analogously to Eq. (13-4). Expressing Eq. (13-8) in words, we have the following theorem: *If the device is operating at X_E, which would be an equilibrium point if the supply voltage were V_E, but if in reality $V = V_S$, then di/dt is positive if $V_S > V_E$. Alternatively, if $V_S < V_E$ then di/dt is negative.* Let us apply this principle to Fig. 13-7*b*. Consider, for example, load line 1, which intersects the NR characteristic at X. Is this a point of stable or unstable equilibrium? If a disturbance takes the circuit to point X_1, then since

$$V_S = V > V_1 = V_E$$

di/dt is positive. Hence, the operating point X_1 must move in the direction of increasing current, away from X and toward A. This argument establishes that X is an unstable point. Hence, if the circuit is adjusted to have a load line such as 1 in Fig. 13-7*b*, it will operate in an astable mode. Applying the above principle to the conditions depicted by load line 2, we can verify that Y is a stable point.

Second, we recognize that Fig. 13-8 gives the equivalent circuit from which to calculate the response to small perturbations. Again we have a one-time-constant circuit which will yield a response of exponential form $\epsilon^{-(R-R_n)t/L}$. The exponent will be positive (unstable case) if $R_n > R$ (load line 1) and negative (stable case) if $R_n < R$ (load line 2). The reverse condition applies for a current-controlled device since in Sec. 13-5 we find that a stable point corresponds to $R_n > R$.

We may note that to ensure stability of equilibrium point on the NR portion of the characteristic, no matter how large R_n may be, we require that R be arbitrarily large. Hence the present case is "open-circuit stable," in comparison with the previous circuit which was "short-circuit stable."

A basic difference between the present voltage-controlled device and the previously discussed current-controlled case is seen in the discontinuous jumps B to B' and A to A'. In the present case the jumps are changes in voltage, whereas in the previous circuit current discontinuities were encountered. It is the reactive element which was added to the circuit (the inductor in the voltage- and the capacitor in the current-controllable-device circuit) which determines the type of abrupt transition. As we shall see, the time intervals established in the monostable and astable circuits are determined by this reactive element. In the bistable circuit, where no timing interval is to be

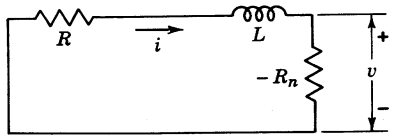

Fig. 13-8 Equivalent circuit for calculating response of circuit of Fig. 13-7*a* for small excursions in the negative-resistance region.

established, the addition of a reactive element is theoretically unnecessary. However, it is found in Sec. 13-10 that an improvement in the transition time results if a small amount of reactance is added in some circuits: for example, a small inductance in series with a tunnel diode.

The remainder of this chapter makes use of the principles enunciated above to explain the operation of switching circuits using the NR devices discussed in the preceding chapter. Calculations of the timing intervals established in monostable and astable waveforms and of the transition time in a bistable circuit are also given.

13-7 TUNNEL-DIODE MONOSTABLE CIRCUIT[2,3]

A monostable tunnel-diode circuit is shown in Fig. 13-9. Bias is provided by the source V in Fig. 13-9*a*, which is adjusted so that the load line intersects the characteristic at one point on the positive-resistance portion. The operating point is initially at point O, where $v = V_o$ and the diode current is $i = I_o$. A positive voltage pulse v_s is applied to raise the load line so that it clears the peak at A. This trigger must have a time duration t_p adequate to allow the current in the inductor to change from I_o to I_P. The operating point having been raised to A, the circuit, of its own accord, follows the path indicated by the arrows, returning eventually to the starting point at O.

Waveforms of output voltage and diode current, somewhat idealized, are shown in Fig. 13-10. The application of the voltage pulse carries the diode from O to A, increasing the voltage from V_o to V_P and the current from I_o to I_P. If the pulse amplitude were large enough so that the asymptotic limit to which the current were headed was much larger than I_P and if the diode resistance in the range from O to A were constant, then the rise of voltage from O to A would be linear as shown.

At A the voltage jumps abruptly to B, where the voltage is V_F, while the current remains constant at I_P. As the operating point now moves from B to C, the voltage drops from V_F to V_V and the current from I_P to I_V. If the

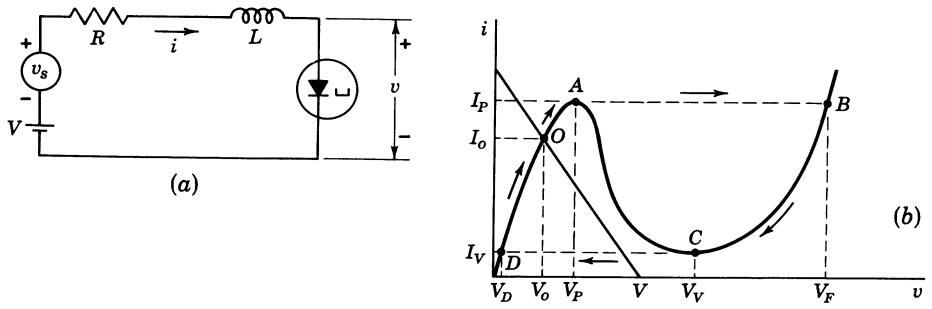

Fig. 13-9 Monostable operation of a tunnel-diode (*a*) circuit, (*b*) operating path.

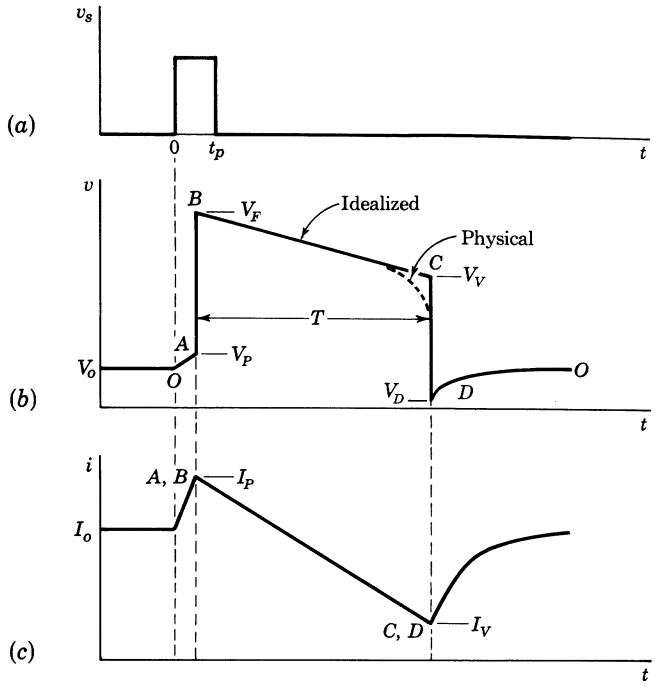

Fig. 13-10 Waveforms of monostable tunnel-diode circuit. (*a*) Triggering pulse; (*b*) output voltage; (*c*) tunnel-diode current.

pulse persisted indefinitely, the load line would establish a stable equilibrium point on the high-voltage positive-resistance portion of the characteristic somewhat below B. We have assumed, however, that long before this equilibrium point is approached the pulse has terminated. Hence the operating point continues from B to C. There is then an abrupt transition in voltage from V_V to V_D at point D, and finally the circuit settles down to initial point O in an asymptotic manner.

If the diode characteristic in the region from B to C were approximated by a constant resistance, the waveform between these points would be exponential and could be readily calculated (see below). We have represented, as an approximation, that the current falls linearly. Since the resistance increases as the operating point moves from B to C, then the time constant L/R decreases as C is approached. Hence, in a physical circuit, the principal respect in which the voltage waveform differs from that of Fig. 13-10*b* is that the negative slope increases in magnitude as point C is approached, as is shown by the dashed waveform. Also, of course, the voltage rise from V_P to V_F is not instantaneous but is determined by the time required to charge any shunt capacitance present.

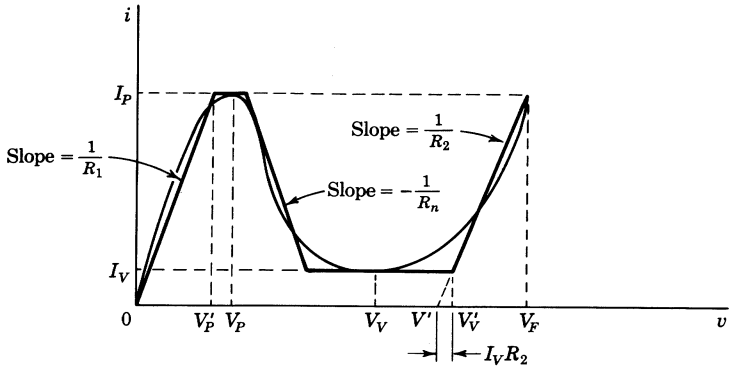

Fig. 13-11 A piecewise linear approximation to a tunnel-diode characteristic (Ref. 2).

A calculation of the duration T of the quasi-stable state, which agrees with experiment[2] to within about 10 percent, can be easily carried out if the tunnel-diode characteristic is represented by the piecewise linear approximation of Fig. 13-11. A reasonable fit with the tunnel-diode curve is obtained if we choose

$$V_P' = 0.75V_P \qquad \text{and} \qquad V_V' = \frac{V_F + V_V}{2} \tag{13-9}$$

If the diode resistance of the portion passing through the origin is called R_1 and if the second positive-resistance region is designated by R_2, then

$$R_1 = \frac{V_P'}{I_P} \qquad \text{and} \qquad R_2 = \frac{V_F - V_V'}{I_P - I_V} \tag{13-10}$$

The line with the negative slope is drawn so as to form a reasonable approximation to the NR segment. Fortunately, neither its location nor its slope affects the delay time T.

To calculate T, the time duration from I_P to I_V, we replace the device by a resistor R_2 in series with a battery $V' \equiv V_V' - I_V R_2$ (as dictated by the piecewise linear approximation of Fig. 13-11). The equivalent circuit is now indicated in Fig. 13-12*a* and *b*, which are equivalent since

$$R_T \equiv R + R_2 \qquad V_Y \equiv V' - V = V_V' - V - I_V R_2 \tag{13-11}$$

Let us shift the time origin so that $t = 0$ when $i = I_P$. If the circuit of Fig. 13-12*b* were valid indefinitely, then at $t = \infty$, $i = -V_Y/R_T$. Since this is a single-time-constant circuit,

$$i = -\frac{V_Y}{R_T} + \left(I_P + \frac{V_Y}{R_T}\right)\epsilon^{-R_T t/L} \tag{13-12}$$

Since i decreases to I_V at $t = T$ we can solve this equation to obtain

$$T = \frac{L}{R_T} \ln \frac{V_Y + I_P R_T}{V_Y + I_V R_T} \tag{13-13}$$

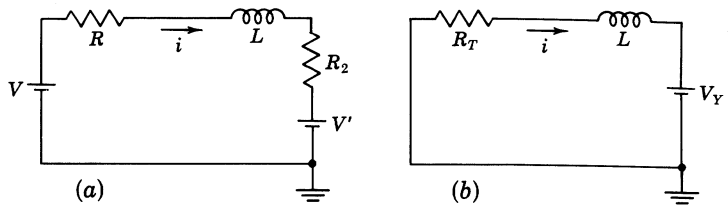

Fig. 13-12 (*a*) In the region from B to C where the current decreases from I_P to I_V the tunnel diode is replaced by a battery V' in series with a resistor R_2; (*b*) simplified circuit.

It is clear that the apparently linear decay in Fig. 13-10 is really exponential. Note that the delay time T is proportional to L. A rough idea of the inductance needed for a desired value of T can be obtained by using the following reasonable order of magnitudes: $V_Y = 0.25$ V, $I_P = 5$ mA, $I_V = 0.5$ mA, and $R_T = 100\ \Omega$. We find $T \approx 0.01L$, so that for $L = 100\ \mu$H, $T = 1.0\ \mu$sec.

If it should be true that $I_P R_T \ll V_Y$, then T is independent of the resistance R_T. To verify this statement we write Eq. (13-13) in the form

$$T = \frac{L}{R_T} \ln\left(1 + \frac{I_P R_T}{V_Y}\right) - \frac{L}{R_T} \ln\left(1 + \frac{I_V R_T}{V_Y}\right) \approx \frac{L}{R_T}\left(\frac{I_P R_T}{V_Y} - \frac{I_V R_T}{V_Y}\right) \tag{13-14}$$

where use has been made of the expansion $\ln(1 + x) \approx x$. Hence

$$T \approx \frac{L(I_P - I_V)}{V_Y} \tag{13-15}$$

The recovery time constant at the end of the waveform is $L/(R_1 + R)$.

A tunnel-diode one-shot which allows one side of the trigger source to be grounded is shown in Fig. 13-13. Additionally, the voltage division through

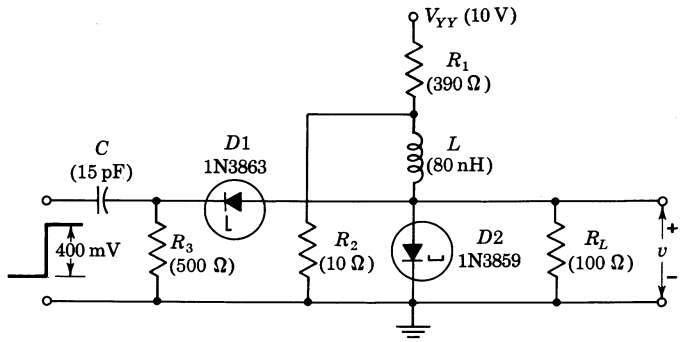

Fig. 13-13 A tunnel-diode monostable multivibrator which allows the trigger source to be grounded. Typical values are shown for components, supply voltage, and triggering-signal amplitude. (Courtesy Radio Corporation of America.)

the resistors R_1 and R_2 provides the small supply voltage required for proper bias of the diode even from a relatively large 10-V supply. The quiescent voltage across the diode is only about 250 mV and the input trigger only 400 mV in amplitude. For this reason the input trigger is introduced through a backward diode $D1$ (Sec. 12-2).

13-8 TUNNEL–DIODE ASTABLE CIRCUIT

In Fig. 13-14*a* the supply voltage and load line have been selected to yield an equilibrium point at O. This point is unstable, and the operating point having moved, say, to point A, it will thereafter follow the circuital path indicated by arrows. Waveforms of diode voltage and diode current are shown in Fig. 13-14*b* and *c*. Again these waveforms have been idealized somewhat. If the diode characteristic were piecewise linear the rises and falls of voltage and current in the waveforms would be exponential. In a physical circuit the voltage waveform departs from the idealized waveform much in the manner shown in Fig. 13-10.

The tunnel-diode astable-circuit waveform is not necessarily exactly symmetrical ($T_1 \neq T_2$) because the portions DA and BC of the device characteristic are not identical. On the other hand, the two portions of the cycle are often not markedly different.

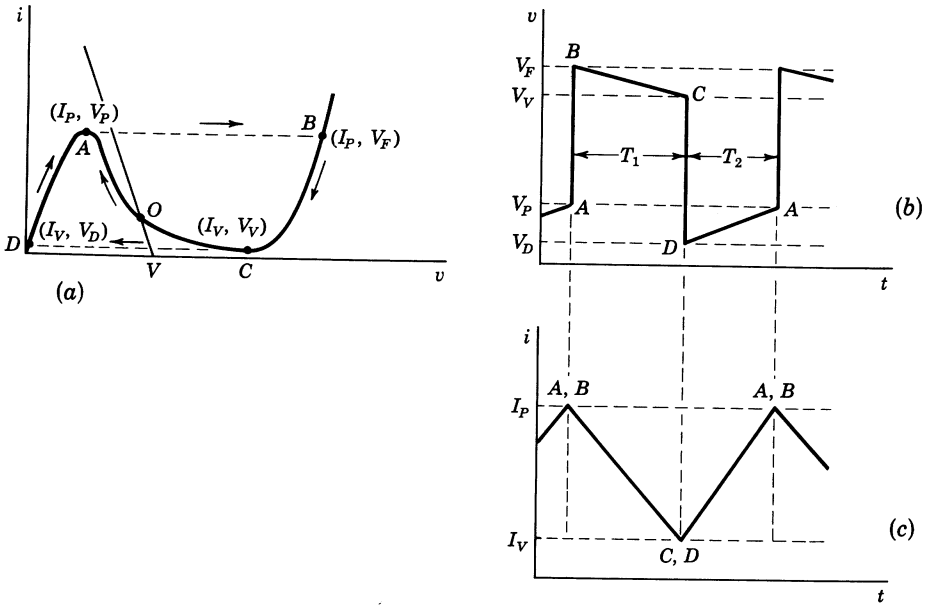

Fig. 13-14 Tunnel-diode astable multivibrator. (*a*) Adjustment of load line; (*b*) voltage waveform; (*c*) current waveform.

Using the piecewise linear approximation of Fig. 13-11, the time T_1 is given by Eq. (13-13). The expression for T_2 will now be found. In the range from D to A, where the current increases from I_V to I_P, the diode may be replaced simply by a resistor R_1. Hence the equivalent circuit of Fig. 13-12*b* is applicable if $V_Y = -V$ and R_T is replaced by

$$R_T' \equiv R + R_1 \tag{13-16}$$

where R is the load resistance. Proceeding as we did in deriving Eq. (13-13), the duration T_2 of the second portion of the waveform is found to be given by

$$T_2 = \frac{L}{R_T'} \ln \frac{V - I_V R_T'}{V - I_P R_T'} \tag{13-17}$$

The total period is $T_1 + T_2$ and the free-running frequency is the reciprocal of this time. For the parameters given in the preceding section and for a symmetrical waveform the frequency of oscillation is $f = 0.5$ MHz for $L = 0.1$ mH, and f varies inversely with L.

If a square wave of the form shown in Fig. 13-14*b* is required with the exception that the tilt is not acceptable, such a waveform may be generated by using the astable tunnel-diode circuit to drive a bistable tunnel-diode circuit. Thus, if the waveform of Fig. 13-14*b* is differentiated with a small RC time constant and if the resulting spikes (alternatively positive and negative) are applied to the flip-flop circuit of Sec. 13-10, an excellent square wave is obtained.

13-9 TUNNEL–DIODE COMPARATOR[4]

A comparator or discriminator (Sec. 7-11) is a circuit which yields an abrupt response when a critical reference voltage or current is attained by a waveform. A tunnel-diode comparator circuit is shown in Fig. 13-15. Bias is provided by the voltage source V in Fig. 13-15*a* or the current source I in Fig. 13-15*b*, corresponding to which is the load line 1 in Fig. 13-15*c* joining I to V with slope $-1/R$. Consider that the initial equilibrium point is at X. When the signal v_s or i_s raises the load line to position 2, where it just clears the peak of the tunnel-diode characteristic, an abrupt transition to V_F will take place and then the diode will settle to the equilibrium point X'. The abrupt transition in output voltage from V_P to V_F constitutes the sharp comparator response. The signal current i_s in Fig. 13-15*b* at which the comparator responds is $I_P + V_P/R - I$, and the corresponding signal voltage v_s in Fig. 13-15*a* is $V_P + RI_P - V$.

The tunnel-diode comparator is fundamentally different from the diode comparator discussed in Sec. 7-13. In the rectifying diode comparator the output-voltage change is, at most, equal to the input-voltage change, and comparator action is obtained by suppressing the input signal until the diode

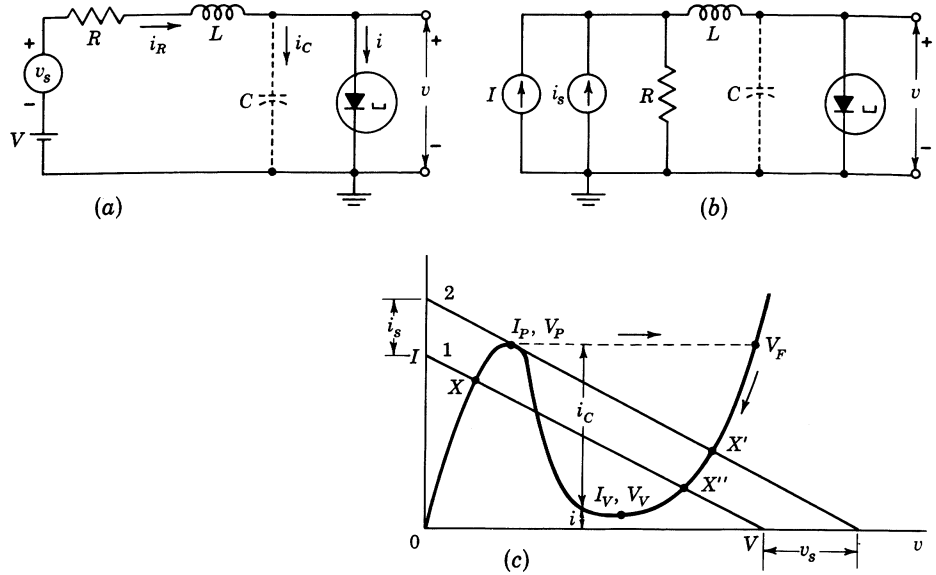

Fig. 13-15 The tunnel diode used as a comparator. In (*a*) and (*b*) the sources are represented by Thévenin's and Norton's equivalents, respectively. (c) Illustrating the abrupt response when the load line just clears the peak of the characteristic.

passes through its break point. In the tunnel-diode comparator the output response bears, in principle at least, no relationship to the change of input signal required to activate the comparator. Ideally, the most insignificant change in input voltage produces a change $V_F - V_P$ in the output. Even with physical tunnel diodes the energy required to carry the comparator from one side to the other is remarkably small, being of the order of 10^{-15} J (a pulse 5 mV in amplitude of 2 nsec duration in a 50-Ω load dissipates 10^{-15} J).

The speed of transition of the comparator is of interest. The speed is limited by the inherent junction capacitance of the tunnel diode, which appears dashed in Fig. 13-15*a* and *b*. Let us assume that the effect of the inductance predominates in the circuit, so that we may reasonably make the approximation that the inductor current remains constant ($i_R = I_P$) in spite of the presence of the capacitance C. From Fig. 13-15*c* we see that, over most of the transition, the diode current i is much smaller than the capacitive current i_C. If we neglect i altogether compared with i_C, then the capacitor charges at a constant current I_P, and since the capacitor voltage changes by $V_F - V_P$ the time of transition is $t_r = C(V_F - V_P)/I_P$. The value of $V_F - V_P$ is approximately 0.5 V for germanium and about 1 V for gallium arsenide. We have then

$$t_r = \frac{C}{2I_P} \quad \text{for Ge} \qquad t_r = \frac{C}{I_P} \quad \text{for GaAs} \tag{13-18}$$

Manufacturers normally specify I_P/C as a figure of merit for tunnel diodes in connection with switching applications. Typical transition times are in the range of a few nanoseconds down to possibly 0.1 nsec in an extreme case.

13-10 TUNNEL-DIODE BISTABLE CIRCUIT

With the load line selected as in Fig. 13-15*c* the circuit has two stable states at the points of intersection of the load line with the positive-resistance portions of the device characteristic at X and X''. If the circuit is at X and the signal source furnishes a *positive* pulse adequate to raise the load line to position 2, a transition will occur, and when the pulse has passed, the circuit will find itself at X''. Similarly, a *negative* pulse adequate to drop the load line to the point where it clears the bottom of the characteristic will reset the circuit to its original stable point at X. Thus the circuit has two permanent stable states and may be used to store binary information or for any of the other purposes for which binary devices are employed.

Suppose that we desired to trigger the tunnel-diode flip-flop with a train of pulses (of alternating polarity) at the maximum possible rate. The minimum time between pulses must be the sum of the transition time t_r and the settling time t_s. The former, which is limited by the shunt capacitance, is the time required to change the voltage from V_P to V_F and was estimated to be of the order of 1 nsec in Sec. 13-9. The time t_s, which is determined by the series inductance, is the time it takes the diode to settle from the voltage V_F to the voltage at X'' in Fig. 13-15*c*. If the current at X'' is $I_{X''}$, then i decreases exponentially from I_P to $I_{X''}$ with a time constant $\tau = L/R_T$. We shall assume, as we did in Sec. 10-5 in connection with the transistor binary, that $t_s \approx 2\tau = 2L/R_T$. For $R_T = 200\ \Omega$, $t_s = 0.01L$. If the settling time is to be no longer than the transition time of 1 nsec, then L must not exceed 100 nH.

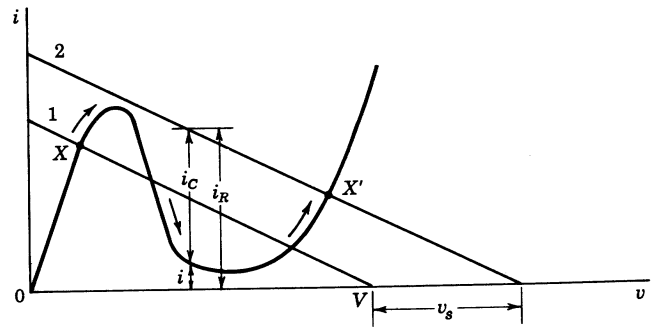

Fig. 13-16 Tunnel-diode bistable operating path if no series inductance is present.

Since t_s is proportional to L and we want t_s to be as small as possible, why not omit L altogether? We shall now show that if no inductance is added to the circuit it will still possess bistable properties but that t_r will be increased. Consider the circuit of Fig. 13-15 but with $L = 0$. The operation is indicated in Fig. 13-16. With $v_s = 0$ load line 1 is applicable and the quiescent point is X. Then an input step is applied and the load line moves to position 2. The steady-state condition is at X', but since the operating point must not leave the tunnel-diode characteristic for any finite interval then it must move from X to X' along the curve, as indicated by the arrows. The time to charge the shunt capacitance is

$$t_r = \int_{V_X}^{V_{X'}} \frac{C\,dv}{i_C} = \int_{V_X}^{V_{X'}} \frac{C\,dv}{i_R - i} \tag{13-19}$$

where i_C, i_R, and i are indicated in Fig. 13-16. In general the integration must be carried out graphically. If a piecewise linear approximation is used for the diode characteristic, then t_r can be evaluated analytically (Prob. 13-22). In Fig. 13-15*c*, i_C equals the difference between I_P and the diode current i. In Fig. 13-16, i_C equals the difference between the current on the load line corresponding to v and the diode current. We see that i_C is smaller in Fig. 13-16. Hence, t_r will be larger (perhaps by a factor of 2) if no inductor is used in the circuit. Therefore, a small amount of inductance should be added to the circuit so that the rise time may be improved without appreciably increasing the settling time. The required value of inductance is best found experimentally, but the above arguments indicate that a reasonable value to start with is of the order of 100 nH. Of course, the larger the triggering signal v_s, the larger will be i_C and the smaller t_r, and hence the necessity for adding inductance decreases as v_s increases.

13-11 TUNNEL-DIODE—TRANSISTOR HYBRID CIRCUITS[2,3]

A tunnel diode has two qualitites of great merit in switching applications It switches extremely rapidly ($\approx$ 1 nsec) and responds to a pulse of very small energy. We noted earlier that a pulse of 10^{-15} J could be counted on to move the tunnel diode past a critical point and initiate a transition. In comparison, a transistor may require a pulse of 10 times larger energy to switch states. Moreover, a single tunnel diode may be used to construct a circuit with two stable states, whereas two transistors are required for this purpose.

On the other hand, a transistor has the advantage over the tunnel diode that the transistor operates at appreciably higher voltages. The voltages and voltage changes encountered in tunnel diodes are of the order of a few tenths of a volt, but in transistor circuits these voltages are at least tens of volts. Additionally, the tunnel diode has the very disconcerting feature that, having only two terminals, the input and output ports are not isolated from one another. As a consequence, in circuits that involve cascades of tunnel diodes, it is difficult to ensure that the signal will proceed in one direction only. It is not surprising, then, that advantages accrue from the employment of combinations of tunnel diodes and transistors in circuits that exploit the merits of each device.

A basic *hybrid* circuit is shown in Fig. 13-17*a*. In Fig. 13-17*b* are plotted the tunnel-diode characteristic (i_N against v), the input characteristic of the transistor (i_B against v), and the composite characteristic ($i = i_N + i_B$ against v). We observe that the composite input characteristic of the hybrid tunnel-diode–transistor combination retains the general shape of a tunnel-diode characteristic. That this feature persists depends on the fact that a germanium transistor is being employed. For in a germanium transistor the base current becomes appreciable in comparison with the diode current at forward voltages of the order of 0.2 V. This voltage, as indicated in Fig. 13-17*b*, falls normally between the peak and valley of a tunnel diode (Table 12-1). If a silicon transistor had been used, the transistor would not yet be turned ON even when the tunnel diode were operating well up on the high-voltage positive-resistance portion of its characteristic. It is, however, possible to use hybrid circuits with silicon transistors by returning the cathode of a tunnel diode to a positive voltage of some tenths of a volt. In this way the tunnel-diode characteristic will be shifted in the direction of positive voltage to the point where the rising base current crosses the tunnel-diode characteristic between its peak and valley. Either a Ge or GaAs tunnel diode may be used.

Since the input characteristics of the hybrid circuit and the tunnel diode have the same form, we may use this input characteristic for all the same types of switching functions. Thus the load line in Fig. 13-17*b* is appropriate for flip-flop operation, and the hybrid circuit of tunnel diode and transistor together operates as a bistable device. To drive a transistor from cutoff to saturation requires that the input current increase from nominally zero to some hundreds of microamperes. Observe, then, that as required, the base current corresponding to point X, the lower voltage of the two stable points, is

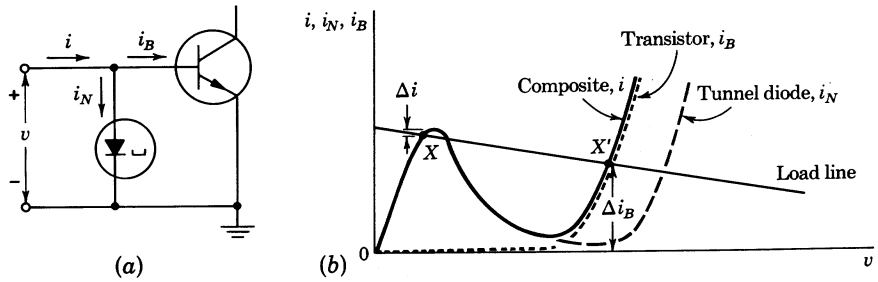

Fig. 13-17 (*a*) A basic tunnel-diode–transistor hybrid circuit; (*b*) composite characteristic formed by combining individual characteristics of tunnel diode and transistor.

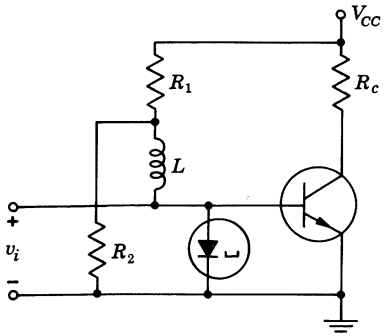

Fig. 13-18 A hybrid circuit which may be adjusted to function as a comparator or to operate in an astable, monostable, or bistable mode.

negligible, and at X', the other stable point, the base current may be comparable to the peak current I_P. Observe, further, that the tunnel diode provides *current gain* at wide bandwith between the circuit input and the base. A change in current Δi at the input triggers the circuit to point X', and the corresponding change in i_B is Δi_B as shown. In principle, by setting point X arbitrarily close to the peak, we may increase the current gain without limit. Of course, as a matter of practicality, requirements for stability against aging, temperature changes, noise, etc., will establish some minimum separation between X and the peak.

Now a second transistor substituted for the tunnel diode would have provided the current gain just as well. The use of a second transistor, which involves additional components and a more complicated coupling arrangement, would have lost for us the delightful simplicity of the hybrid circuit. But, putting this relatively unimportant matter aside, let us compare the responses to an input switching signal of a cascade of transistor stages and a cascade of hybrid circuits. Suppose that in a cascade of transistors a step of current or voltage of zero rise time is applied to the first transistor. The output of the first transistor will have a finite rise time. This finite-rise-time signal applied to the second transistor will cause the output of the second transistor to have an even longer rise time, and so on. However, the speed of transition of a tunnel diode is nominally not influenced by the speed of the applied signal, because the signal does not drive it from one state to another but only acts as a trigger. Since, also, the speed of tunnel diodes is comparable to or faster than even the highest-speed transistors, the interposition of tunnel diodes between transistors serves in effect to keep the speed and amplitude of the drive signal at each transistor base adequate to cause the transistor to respond at its fastest speed.

A basic circuit which can be adjusted to function as a comparator or to operate in a bistable, monostable, or astable mode is shown in Fig. 13-18. The load line at the input passes through an equivalent supply voltage $R_2V_{CC}/(R_1 + R_2)$, and the equivalent load resistance is the parallel combination of R_1 and R_2. Thus we may adjust the load line to intersect the hybrid input characteristic in whatever manner is appropriate to attain the

type of operation desired. The terminals at the left are for a triggering signal when required. The circuit of Fig. 13-18 is that of Fig. 13-13 with the load R_L across the tunnel diode replaced by the base circuit of the transistor.

The hybrid-circuit multivibrators have an advantage over the two-transistor multivibrators with respect to responding to a narrow triggering pulse. When, in a two-transistor multivibrator, a pulse is applied, say at the base of one transistor, to induce a transition, the pulse must persist long enough to allow the collector current to change substantially so that a transition takes place. Otherwise, at the termination of the pulse the multivibrator will simply settle back into its original state. In the hybrid circuit the pulse need only last long enough to get the load line to clear the peak or valley of the characteristic. If the pulse lasts long enough to get the tunnel diode irreversibly started to its other state the transition is ensured. Even if the collector current has, in this time, not changed appreciably, it does not matter. The collector current will catch up later.

13-12 CIRCUIT APPLICATIONS OF *p-n-p-n* DIODES[5]

A *p-n-p-n* diode (Secs. 12-4 and 12-5) may be operated in an astable, monostable, or bistable mode, depending, as we have seen, on the relationship of the load line to the device characteristic. In some cases, for the sake of the waveforms thereby generated or for convenience in triggering, two *p-n-p-n* diodes are used rather than one.

Sawtooth Generator The circuit of Fig. 13-19*a*, when adjusted for astable operation, generates the waveform in Fig. 13-19*b*. This "sawtooth"-type waveform (which may be generated by any current-controlled device) finds extensive use in timing applications and will be discussed in detail in Chap. 14. To consider the operation of Fig. 13-19 we disregard, for the moment, the

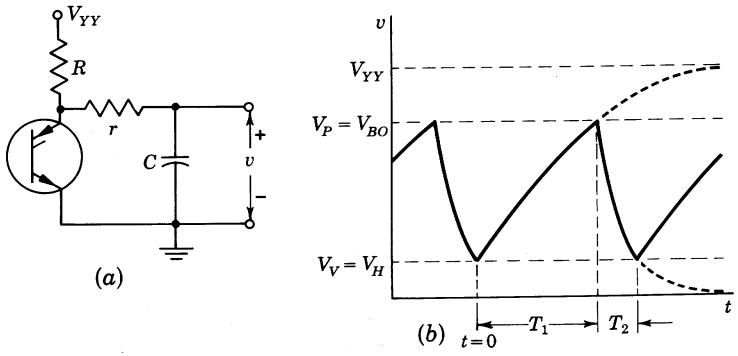

Fig. 13-19 (*a*) A *p-n-p-n* diode sawtooth generator; (*b*) output waveform.

small resistance r and assume that the capacitor is initially uncharged. Since the voltage across the diode is low, the device is in its nonconducting state, so that the current supplied by V_{YY} flows through R into the capacitor. The capacitor charges toward V_{YY} until the output voltage reaches V_{BO}, the breakover voltage of the diode. At this peak $V_P = V_{BO}$, the device switches abruptly to its high-current–low-voltage state and the capacitor discharges through the diode. The diode remains in this state until the capacitor has discharged to the voltage V_H, where it can no longer supply the holding current. From the minimum or valley voltage $V_V = V_H$ the diode then returns to its OFF state and the cycle repeats. The small resistor r has been included to limit the peak current through the diode to within its rating during the interval of capacitor discharge.

The capacitor charges from an initial voltage V_V exponentially with a time constant $\tau = (R + r)C$ toward V_{YY}. At $t = T_1$ the voltage reaches V_P. Solving for T_1 we find

$$T_1 = \tau \ln \frac{V_{YY} - V_V}{V_{YY} - V_P} \tag{13-20}$$

The fall time T_2 is difficult to calculate since it depends upon the holding current I_H, which is often not specified and which may be quite variable from unit to unit. The capacitor voltage decreases exponentially from V_P toward zero, and the diode becomes nonconducting when its current falls below I_H. Let us assume that a reasonable interval for the current to fall to I_H is three time constants, or $T_2 = 3rC$, a quantity which may be as small as some tens of nanoseconds.

The frequency of the oscillation is $f = 1/(T_1 + T_2)$. This frequency may be increased by decreasing R. However, R was originally selected to intersect the characteristic in the manner indicated in Fig. 13-5. If R is decreased, a point will eventually be reached where the intersection occurs on the high-current positive-resistance portion of the characteristic. The circuit then latches, with a stable point in the high-current region. This manner of operation is to be avoided on the grounds that the continuous ON current will ordinarily exceed the allowed average diode current. After R has been decreased just short of moving the equilibrium point out of the negative-resistance region, the frequency may be increased further by reducing C. With a physical diode we find that when the capacitance C is progressively decreased to the point where the time constant becomes comparable to the time intervals required for the diode to make transitions between states, the sawtooth waveform looks rather more sinusoidal. Also, the oscillation amplitude decreases with increasing frequency.

Pulse Generator The circuit of Fig. 13-19 may be used as a pulse generator since, each time the capacitor discharges abruptly, a pulse of voltage appears across r. When intended as a pulse generator the load resistance is larger than the small resistance r used to limit the current and is located, as

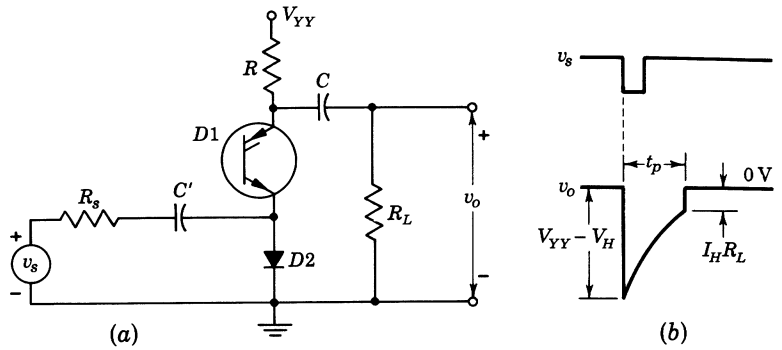

Fig. 13-20 (*a*) A *p-n-p-n* diode pulse generator; (*b*) input and output waveforms with $R \gg R_L$.

shown in Fig. 13-20, so that one side of the pulse output may be at ground. The circuit in Fig. 13-20 allows for the possibility of monostable operation. In such operation the supply voltage is adjusted to be somewhat less than the breakover voltage. A negative pulse introduced as indicated increases the voltage across the *p-n-p-n* diode $D1$ to the point where switching occurs. The capacitor discharges, a voltage pulse appears across R_L, and the circuit restores itself to its initial state. In Fig. 13-20*b* the output-pulse width is $t_p \approx 3R_LC$.

When the source v_s applies a negative pulse through C', the *p-n* diode $D2$ is momentarily back-biased while the voltage across $D1$ is raised to the point where it fires. The capacitor C then discharges, the path of the discharge being through $D1$, C', R_s, and R_L. Almost immediately, however, the voltage across R_s and C' rises to the point where $D2$ becomes forward-biased, and thereafter the discharge proceeds through $D2$ rather than the source. The usefulness of $D2$ (rather than a resistor) is that it limits the loading on the pulse source.

The output-pulse waveform starts at ground level. When the diode $D1$ fires, the anode voltage drops from V_{YY} to the holding voltage V_H. This abrupt voltage change is transmitted through C to the output. Since $R \gg R_L$ the diode current and the current through R_L are very nearly the same. This current decreases as the capacitor discharges, until the holding current I_H is reached. At this point diode $D1$ turns OFF abruptly and consequently there is an abrupt voltage change I_HR_L at the output. Although it is true that, in monostable operation, an input pulse is required to produce an output pulse, the output pulse may be larger in amplitude, may be wider, and is available at a much lower impedance level than the triggering pulse.

Bistable Multivibrator In the two previous *p-n-p-n* diode circuits, the circuit operated in an astable and in a monostable mode, respectively. We can also construct a bistable circuit with a single diode, but for the sake of

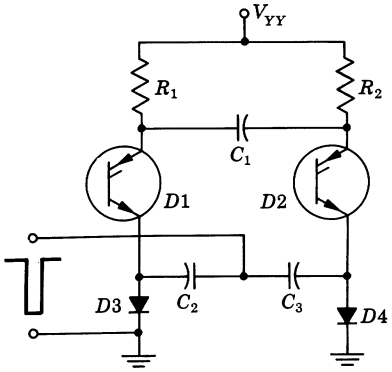

Fig. 13-21 A multivibrator using two p-n-p-n diodes. Nominally $R_1 = R_2$ and $C_2 = C_3$.

convenience of triggering with a pulse of one polarity at one point in the circuit, we use two p-n-p-n diodes.

In the circuit of Fig. 13-21, the supply voltage is less than the breakover voltage and the resistors $R_1 = R_2$ are small enough so that a stable state exists in both the high-current and in the low-current regions. Assume, then, that $D1$ and $D3$ are ON while $D2$ and $D4$ are OFF. The negative pulse, applied to the cathode of $D2$ through C_3, turns $D2$ ON. Consequently, the anode of $D2$ drops abruptly from the supply voltage V_{YY} to the maintaining voltage. This negative step of voltage is applied through C_1 to the anode of $D1$, and $D1$ is thereby turned OFF. The current which flows through C_1 in response to the voltage change at the anode of $D2$ must be supplied through R_1. This resistor R_1 is selected to be large enough so that the supply voltage cannot furnish through it both the capacitor C_1 current and the holding current for $D1$. Successive negative triggering signals will switch conduction back and forth between $D1$ and $D2$.

Other p-n-p-n diode multivibrators using two diodes are given in Probs. 13-27 and 13-28.

13-13 APPLICATIONS OF THE UNIJUNCTION TRANSISTOR[6,7]

A unijunction transistor may be operated in an astable, monostable, or bistable mode depending on the relationship of the load line to the device characteristic.

Sawtooth Generator A relaxation-oscillator circuit, similar in operation to the p-n-p-n diode circuit of Fig. 13-19, is shown in Fig. 13-22. The circuit must be biased for astable operation; that is, the load line determined by V_{YY} and R must intersect the input characteristic in the negative-resistance region. The resistors R_{b1} and R_{b2} are not essential to the circuit but are included because the voltages developed across these resistors may prove useful (see Sec. 14-4). The capacitor C charges to the peak voltage V_P, the device turns ON, and the capacitor discharges to the valley voltage V_V,

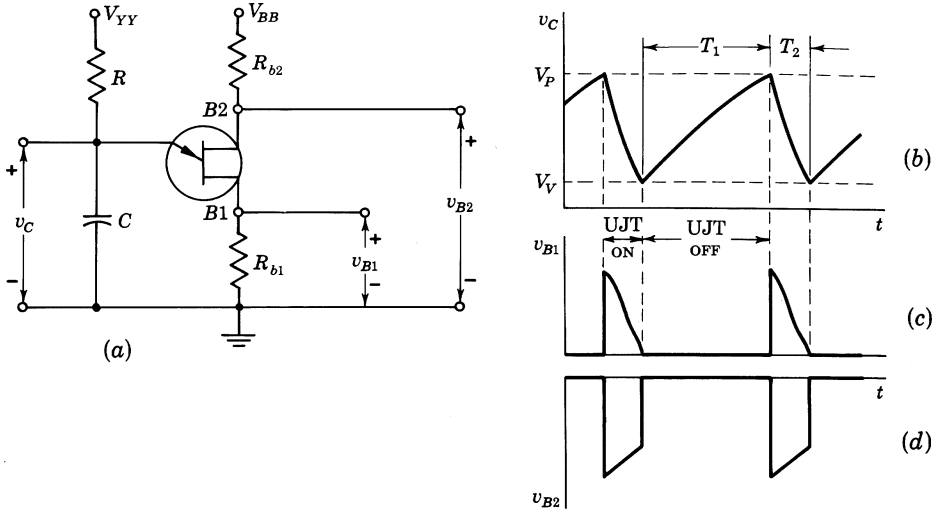

Fig. 13-22 (a) Unijunction transistor sawtooth-waveform generator; (b) capacitor voltage waveform; (c) voltage waveform at $B1$; (d) voltage waveform at $B2$.

whereupon the cycle repeats. The capacitor voltage appears as in Fig. 13-22b. The charging time T_1 is given by Eq. (13-20).

Pulses develop as shown in Fig. 13-22c and d across R_{b1} and R_{b2} during the interval when the device is ON and the capacitor is discharging. The pulse at $B1$ has an abrupt leading edge, but the anticipated abrupt drop at the trailing edge may not be easily apparent if the holding current is small in comparison with the current at the moment of breakdown. The $B2$ current is smaller, being the $B1$ current minus the emitter current, but is more nearly constant during the capacitor discharge. Improved linearity of the triangular waveform may be obtained by using feedback methods, as explained in Chap. 14. An improved pulse waveform is obtained by connecting the base of a CE n-p-n transistor amplifier to $B1$ of Fig. 13-22a and taking the output from the collector of the transistor.

The resistor R_{b1} is in series with the device terminals between which appears the negative resistance. In order that the effect of the negative resistance not be deemphasized it is necessary to limit the magnitude of the positive resistance R_{b1} to some tens of ohms. The resistor R_{b2} may be larger, ranging up to some hundreds of ohms.

Astable Circuit with Controllable ON and OFF Times The total time of a cycle of the circuit of Fig. 13-22 includes the interval during which C discharges. This interval is difficult to control, depending as it does on the characteristics of the device when it is conducting heavily. Such characteristics are ordinarily neither specified nor controlled by the manufacturer. However, for the case where $R_{b1} = 0$ the following empirical relationship has been found[7]

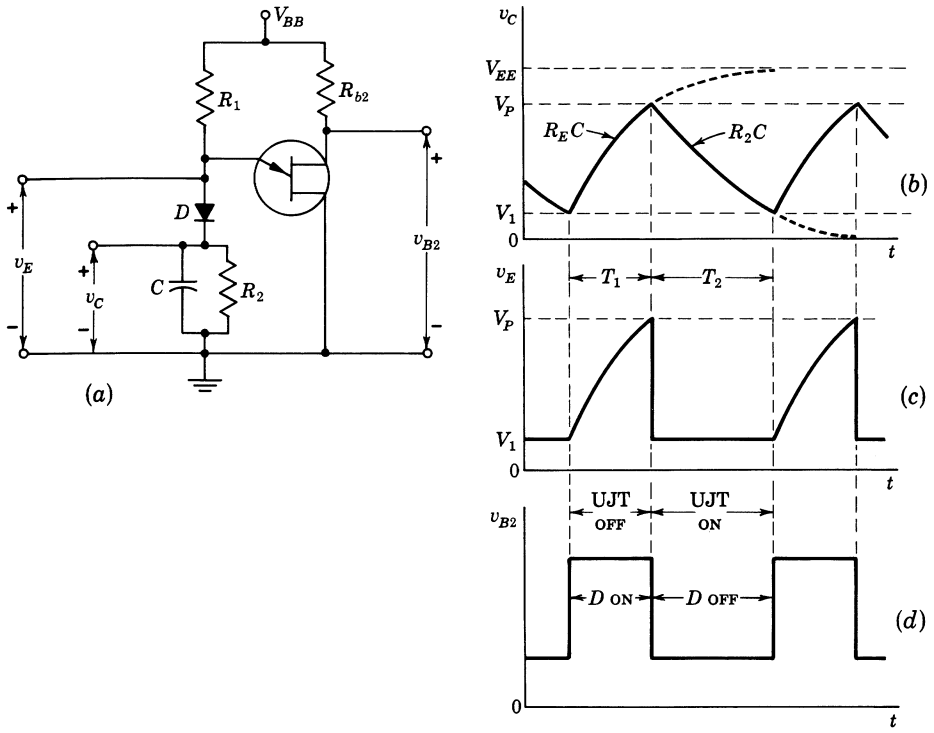

Fig. 13-23 (*a*) Unijunction transistor astable multivibrator yielding two comparable controllable timing intervals; (*b*) waveform across C; (*c*) emitter voltage waveform; (*d*) waveform at $B2$.

for the time T_2 for the emitter voltage to fall from V_P to V_V:

$$T_2 \approx (2 + 5C)V_E(\text{sat}) \tag{13-21}$$

where T_2 is in microseconds, C is in microfarads, and $V_E(\text{sat})$ is in volts. For example, with $C = 0.01$ μF and $V_E(\text{sat}) = 2$ V, $T_2 \approx 4$ μsec. It is also found that T_2 increases with temperature.

A circuit modification which yields a waveform consisting of two comparable controllable intervals is shown in Fig. 13-23. During the interval T_1, when the UJT is OFF, the capacitor C charges through diode D and an effective resistance R_E toward the voltage V_{EE}, where

$$R_E \equiv \frac{R_1R_2}{R_1 + R_2} \qquad V_{EE} \equiv \frac{R_2V_{BB}}{R_1 + R_2} \tag{13-22}$$

if we neglect the forward voltage across the diode. This asymptotic voltage is selected, as indicated in Fig. 13-24, to be larger than the peak voltage, $V_{EE} > V_P$, so that the UJT goes ON when $v_E = v_C = V_P$. At this point the emitter voltage drops abruptly, diode D becomes reverse-biased, and the

capacitor begins to discharge through R_2. During this discharge the voltage v_C is approaching zero asymptotically.

During the interval T_2, when diode D is reverse-biased, the supply V_{BB} furnishes emitter current to the UJT through R_1. The supply V_{BB} and resistor R_1 have been selected, as in Fig. 13-24, so that the point of intersection of the corresponding load line with the device characteristic is in the negative-resistance region at point P_2. In order that this point should be so located it is necessary that

$$R_1 > \frac{V_{BB}}{I_V} \tag{13-23}$$

where I_V is the valley current. The equilibrium voltage is V_1, which is somewhat larger than the valley voltage V_V. Thus, as shown in Fig. 13-23*c*, when the UJT goes ON, v_E falls to V_1. It should be recalled from Sec. 13-5 that even though P_2 is on the NR portion of the characteristic it is a stable equilibrium point, provided that the capacitance C' (not C) shunting the emitter with the diode open is below the critical capacitance.

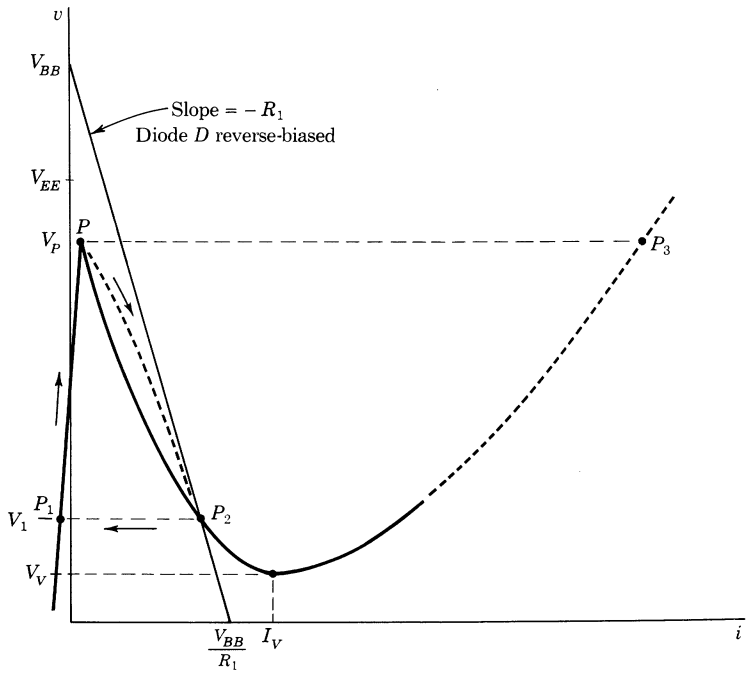

Fig. 13-24 Illustrating the path of operation of the astable unijunction transistor circuit of Fig. 13-23. Note that current is plotted along the abscissa, as in Fig. 12-6, rather than along the ordinate, as in Fig. 13-1*b*.

From Fig. 13-23 we observe that when v_C drops to V_1, diode D conducts, the capacitor C appears again across the negative-resistance terminals, and the point P_2 now becomes unstable. At the moment diode D conducts, the emitter current is diverted through the diode and the UJT goes OFF.

It is of interest to trace the path of operation of the circuit on the volt-ampere characteristic of the device. The characteristic and load lines are shown in Fig. 13-24. Starting at the point P_1, where $v = V_1$, the operating point moves up the characteristic as the capacitor charges until the break point P is reached. In an ideal case (where there is no series inductance L), at this point there would be an abrupt transition at constant voltage to P_3, which is the intersection of the peak current I_P and the characteristic. Thereafter, the operating point would move along the characteristic to the equilibrium point at P_2. Actually, because of the presence of L and the small capacitance C' which shunts the emitter when D is reverse-biased, the transition is not instantaneous. The capacitance C' discharges during the transition and the equilibrium point P_2 is approached by some shorter path, as indicated. In any event, the circuit comes to rest at P_2 and remains at this point until it is rendered unstable by the reconnection of the capacitance C as the diode D becomes forward-biased. At this time a fast transition takes place from P_2 to the initial point P_1, the current through R_1 transferring from the emitter to the diode while the voltage across C remains at V_1.

The charging interval T_1 is given by Eq. (13-20), which now takes the form

$$T_1 = \frac{R_1 R_2 C}{R_1 + R_2} \ln \frac{V_{EE} - V_1}{V_{EE} - V_P} \tag{13-24}$$

The discharge interval T_2 is found from Fig. 13-23*b* to be

$$T_2 = R_2 C \ln \frac{V_P}{V_1} \tag{13-25}$$

The voltage levels of the waveform v_{B2} may be determined by drawing a load line corresponding to V_{BB} and R_{B2} on the characteristics of Fig. 12-7*b*. The OFF level corresponds to the current $I_E = 0$, and the ON level to the current $I_E = (V_{BB} - V_1)/R_1$. Since the emitter current is constant during each of the two intervals, the waveform of Fig. 13-23*d* displays no tilt.

Bistable Circuit[6] A bistable UJT circuit is shown in Fig. 13-25*a*. The use of the two resistors R_1 and R_2 allows some flexibility of adjustment since they make possible separate adjustments of emitter-supply voltage V_{EE} and resistance R_E. That such is the case is seen in Fig. 13-25*b*, where the values of V_{EE} and R_E are given by Eqs. (13-22). The load line passing through the points P_1, P_2, and P_3 corresponds to bistable operation since, of the three stable equilibrium states, only two, P_1 and P_3, are accessible. The load line passing through P_1', P_2', and P_3' may also yield bistable operation. For again, in the absence of capacitance, the point P_3' on the NR portion may

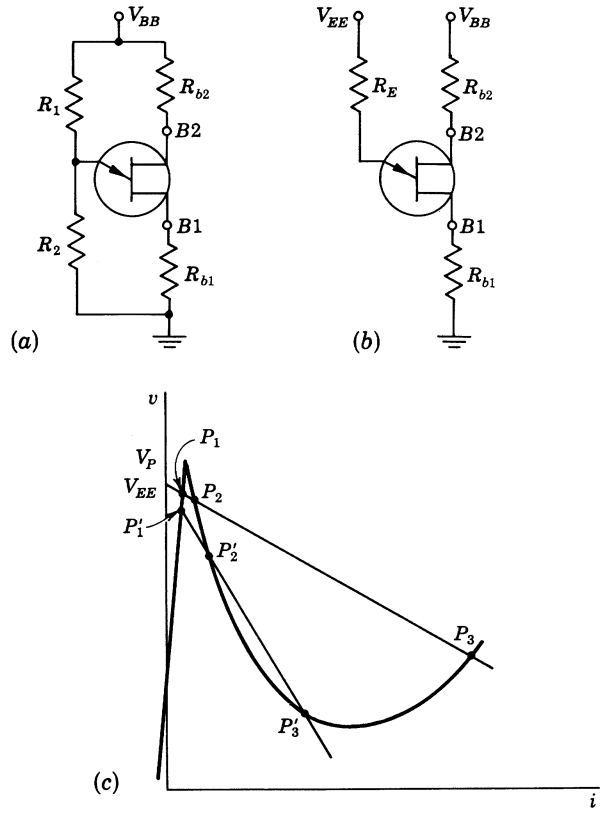

Fig. 13-25 (*a*) A UJT bistable multivibrator; (*b*) circuit equivalent to (*a*); (*c*) two possible load lines which will yield bistable operation.

actually be stable. Note that unlike the astable condition ($V_{EE} > V_P$), it is necessary for bistable operation that $V_{EE} < V_P$.

If the circuit is at point P_1 or P_1', a transition may be induced by raising the voltage at the emitter above V_P. In Fig. 13-25*c* the difference in voltage level between V_{EE}, P_1, and P_1' has been exaggerated. Actually the three voltages are so close that if a triggering voltage in excess of $V_P - V_{EE}$ is introduced either in series with V_{EE} or applied directly to the emitter (say through a small capacitance), then switching will have been accomplished. The circuit may also be triggered by the application of a negative pulse at $B2$. From Eq. (12-1) we see that if the voltage at $B2$ is lowered by ΔV_{B2}, then V_P will be lowered by $\eta/\Delta V_{B2}$. To cause triggering we need to lower V_P by the amount $V_P - V_{EE}$. Thus triggering to the ON condition may be achieved with a negative pulse applied at $B2$ and of magnitude $(V_P - V_{EE})/\eta$, which is larger than that required at the emitter because $\eta < 1$. In the same way a negative pulse at $B1$ of magnitude $(V_P - V_{EE})/(1 - \eta)$ will cause triggering. Observe that at both $B1$ and $B2$ a negative pulse is required.

When the circuit is at P_3 or P_3' a transition may be induced by lowering the load line to the extent that only a single equilibrium point remains, and

this in the low-current region. A negative pulse applied at the emitter will lower the effective V_{EE} and so accomplish switching. Alternatively, a positive pulse at $B1$ will raise the device characteristic and so achieve the same end. In either case the advantage is apparent of operating at P_3' rather than at P_3, since in the former case a smaller trigger will be required. Once the UJT is ON the voltage at $B2$ does not have a marked effect on the forward-biased emitter junction, so that triggering to the OFF state at $B2$ is normally not very effective.

A monostable UJT configuration is given in Fig. 14-8.

13-14 SILICON-CONTROLLED-SWITCH CIRCUITS[8]

All of the circuits which can be designed around *p-n-p-n* diodes and UJTs can be constructed as well with silicon controlled switches. The SCS offers the advantage of a gating terminal. The *p-n-p-n* diode has no separate gating terminal, and any gating voltage to be applied must be introduced as a superposition on the voltage across the two diode terminals. Thus there is no isolation between the triggering source and that part of the circuit which consists of supply voltage, load resistor, and the terminals between which there appears the negative resistance. The situation is not much better with the UJT. Here it is possible to trigger at $B2$ while the negative resistance appears between emitter and $B1$. But we have seen that the triggering pulse required at $B2$ is multiplied by the factor $1/\eta$ (≈ 2) over the trigger required at the emitter. On the other hand, as described in Sec. 12-7, an SCS may be extremely sensitive to a trigger signal on the gate.

A number of applications of the SCS are indicated in Fig. 13-26. In Fig. 13-26*a* an SCS is employed as a comparator. When the signal v_i attains the triggering level, the switch fires and a large and abrupt response occurs in v_o at the output. The firing voltage of the switch has a negative temperature coefficient of about 3 mV/°C. For application over a wide temperature range some form of temperature compensation will be required, such as the use of temperature-sensitive resistors (thermistors) at the input. It should be remembered in this and other applications that the SCS can handle considerable power. Thus the low-level output from a magnetic core or a sensitive transducer applied at the gate in Fig. 13-25*a* can excite power loads placed directly in the anode circuit, for example, a card-punch solenoid, a magnetic clutch, an indicator lamp, etc.

A pulse generator is shown in Fig. 13-26*b*. This circuit is so similar in operation to the circuit of Fig. 13-20 that we need only call attention to the convenience of triggering.

In the sawtooth-generating circuit in Fig. 13-26*c* the capacitor charges through R, and with time both the anode and gate voltage rise to the point where the switch fires. The capacitor then discharges and the cycle begins again.

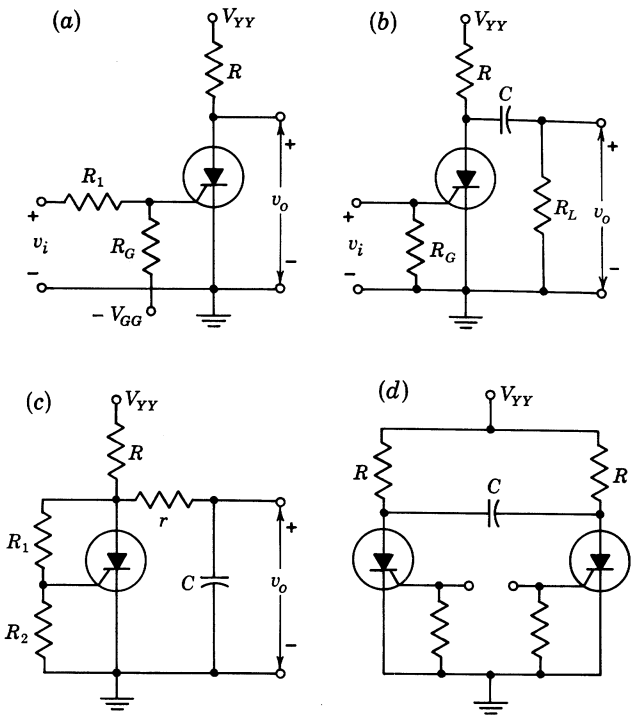

Fig. 13-26 Circuit applications of the silicon controlled switch. (*a*) Comparator; (*b*) pulse generator; (*c*) sawtooth-waveform generator; (*d*) multivibrator or flip-flop.

In Fig. 13-26*d* we have a circuit which may be astable or bistable. It will be astable if the supply voltage is larger than the firing voltage and bistable if the supply voltage is smaller. In the latter case triggering signals will have to be supplied to the two bases through small capacitors, as in the corresponding *p-n-p-n* diode circuit of Fig. 13-21.

13-15 TRANSWITCH, TRIGISTOR, AND THYRISTOR TRIGGERING

We had noted that the principal feature of these devices is the feasibility of turning them OFF with a triggering signal. Two methods of triggering are shown in Fig. 13-27. In Fig. 13-27*a* a positive pulse at the base turns the device ON and a negative pulse OFF. The device is ON for the time interval between the leading edges of the two pulses. In Fig. 13-27*b* both input pulses are negative; one is applied to the base and one to the cathode. As in Fig. 13-20 the diode D allows the device current to flow when it is ON and presents a high impedance to the turn-on pulse when the device is OFF. Applications of these devices in counting circuits are given in Chap. 18.

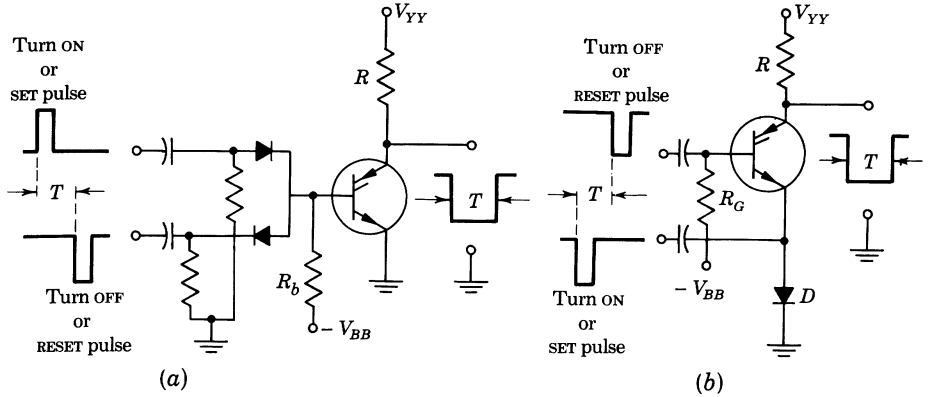

Fig. 13-27 Two methods of triggering a trigistor, transwitch, or thyristor flip-flop.

13-16 AVALANCHE-MODE TRANSISTOR CIRCUITS[9,10]

Most mesa and MADT switching transistors may be used in an avalanche mode as pulse generators. The transistor volt-ampere characteristic of Fig. 6-18 or 6-20 is repeated in Fig. 13-28*a*, and a basic circuit is indicated in Fig. 13-28*b*. The load line is selected to yield a single stable point in the low-current region. The supply voltage charges the capacitor through R_c to a voltage V_{CC} slightly less than the breakdown voltage BV_{CER}. A pulse shown in Fig. 13-28*c* (or some other positive-going signal) applied to the base lowers the breakdown voltage, and the capacitor discharges rapidly through the transistor and the small resistance R_L. The voltage across R_L shown in Fig. 13-28*d* drops very rapidly, as does the collector voltage. The speed with which these voltages change is determined by how quickly the transistor makes the transition from its low-current state to the state in which an avalanche discharge is established. It is in this low transition time (a few nanoseconds) that the transistor excels.

Having reached a peak, the output voltage now decays to zero as the capacitor discharges. The collector voltage, as in Fig. 13-28*e*, starts close to V_{CC} and drops at the same high speed to the latching voltage LV_{CER}, which, as the symbol indicates, is a function of the base resistance. Even after the capacitor has discharged, the collector voltage remains for a time at the latching voltage since an interval is required to allow the transistor to recover and return to its initial state. During this interval a small transistor current flowing now through R_c maintains the collector at the lower voltage. Finally, as the transistor approaches complete recovery, the collector voltage returns again to V_{CC} but at a much slower rate than it fell. We may note, in passing, that if our interest is in a rapid voltage step rather than a pulse we may set $R_L = 0$ and use the collector voltage itself.

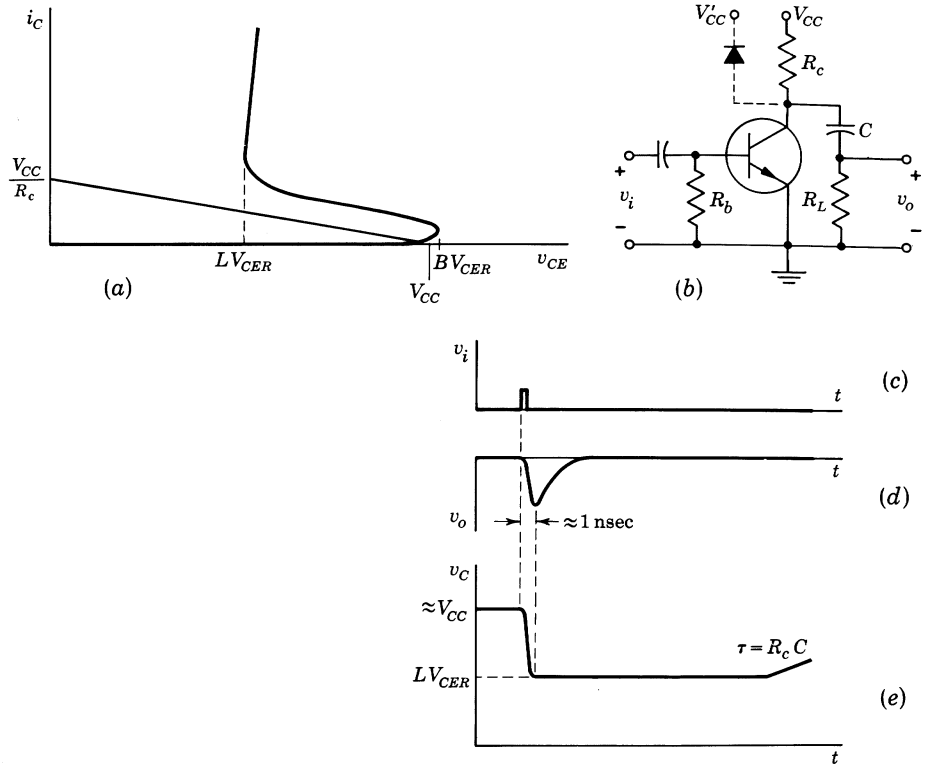

Fig. 13-28 (*a*) Volt-ampere characteristic of avalanche-mode transistor; (*b*) circuit of a pulse generator ($R_L \ll R_c$); (*c*) triggering pulse; (*d*) output waveform; (*e*) waveform at collector.

The pulse width depends upon R_L and C and increases as C increases. The rate at which the circuit may be driven is determined by R_c and C. Typically $R_c \approx 10$ K, whereas $R_L \approx 50\ \Omega$, so that nanosecond pulses with microsecond spacing between pulses may be obtained. Some precautions must be taken when adjusting the circuit for a high repetition rate. If C has been fixed by pulse-width requirements, the repetition rate may be increased by decreasing R_c. But R_c must not be made so small that the transistor will latch and remain permanently in avalanche. Under these circumstances the transistor will exceed its dissipation rating. As noted in Sec. 6-10, latching voltages are in the range of tens of volts and currents in the avalanche region may range up to many hundreds of milliamperes.

A procedure for increasing the repetition rate which avoids the danger of latching is indicated by the diode (shown dashed) in Fig. 13-28*b*. This collector catching diode is returned to a supply voltage V'_{CC} which is less than the breakdown voltage. Thus the supply V_{CC} may be increased well

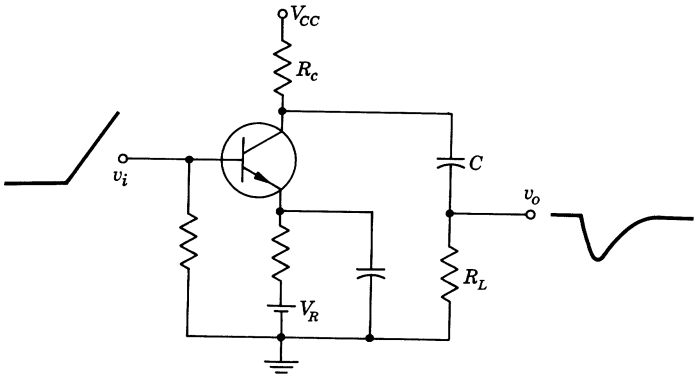

Fig. 13-29 An avalanche-transistor comparator circuit.

beyond the breakdown voltage, thereby increasing the speed of charging of the capacitor and hence the repetition frequency.

A second precaution to be observed also has to do with the transistor dissipation. The maximum frequency of operation is limited by the dissipation rating of the transistor. In physical circuits a 10-MHz repetition frequency is nonetheless possible. The pulse may be made progressively narrower by reducing the size of the capacitor until such time that the pulse width becomes comparable to the rise time. Beyond this point the pulse amplitude will become progressively smaller.

The comparator circuit of Fig. 13-29 constructed with an avalanche transistor is useful for very fast waveforms. A (nanosecond) output pulse is produced when the input exceeds a critical level, which depends upon the reference voltage V_R.

13-17 AVALANCHE TRANSISTOR DELAY-LINE PULSE GENERATOR[10]

An avalanche pulse generator whose pulse amplitude and width are separately controllable and which provides a more rectangular pulse than is available from the circuit of Fig. 13-28*b* is shown in Fig. 13-30*a*. Here the capacitor has been replaced by an open-circuited delay line of characteristic impedance R_o. An equivalent circuit for the purpose of calculating the waveforms is shown in Fig. 13-30*b*, where avalanche breakdown is represented by the closing of the switch S. We now describe the operation of this circuit.

When, in response to a triggering signal, the transistor breaks down (S closes), a negative voltage step $\Delta v = -V$ is applied to the line through the resistor $R_L \ll R_c$. This step has an amplitude $V = V_{CC} - LV_{CER}$. Since the initial line current is zero, then a current step

$$i(0+) = \frac{-V}{R_o + R_L} \equiv I \tag{13-26}$$

starts down the line at $t = 0+$. When this current wave reaches the end of the line at $t = t_d$ it is reflected as a current step $-I$ (the reflection coefficient ρ for current at an open circuit is -1). At $t = 2t_d$ this step $-I$ reaches the beginning of the line and, as indicated in the reflection chart of Fig. 13-30*c*, is again reflected as $(-I)\rho'$, where ρ' for a current wave is the negative of the reflection coefficient for a voltage wave given in Eq. (3-42). Hence, the total line current at $t = 2t_d+$ is

$$i(2t_d+) = I - I - I\rho' = -I\rho' = \frac{-V}{R_o + R_L}\frac{R_L/R_o - 1}{R_L/R_o + 1} \tag{13-27}$$

Neglecting the small current through R_c, we see from Fig. 13-30*b* that the transistor collector current i_C is the negative of the line current i. Hence, the collector current will be positive at $t = 2t_d+$ as long as $R_L > R_o$. Under these circumstances the transistor remains ON and further reflections take place. This mode of operation is undesirable because the waveform across R_L will consist of a series of different voltage levels separated by intervals $2t_d$, rather than a pulse output.

We note from Eq. (13-27) that if $R_L = R_o$ (the line is matched at the input end), then at $t = 2t_d$ the transistor current i_C is brought to zero and consequently the transistor goes OFF and the switch S is opened. However, if $R_L < R_o$, then Eq. (13-27) indicates a reversal of collector current. Actually, in this case the transistor will again simply go OFF. In either case, then, $R_L = R_o$ or $R_L < R_o$, S opens at $t = 2t_d$, and any current through R_L must now flow as well through the resistor R_c, which is very large in comparison with R_L. Therefore the voltage v_o across R_L will drop nominally to zero and remain there. Altogether, we have the result that for $R_L \leq R_o$ there will develop across R_L a pulse whose duration $2t_d$ is controllable through adjustment of the transmission-line delay time and whose amplitude is adjustable through R_L and V in accordance with the relationship

$$v_o = i(0+)R_L = \frac{-VR_L}{R_o + R_L} \tag{13-28}$$

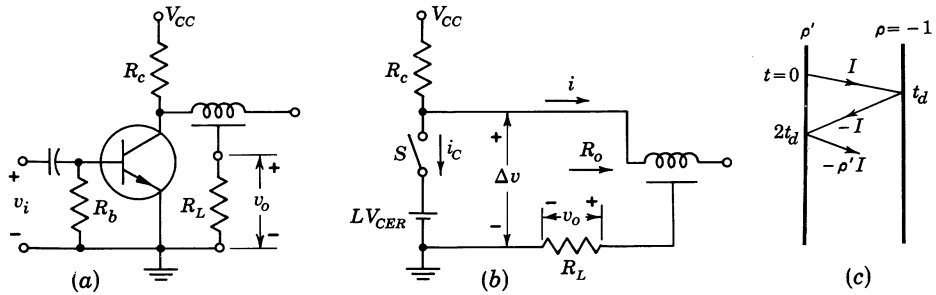

Fig. 13-30 (*a*) The pulse width of an avalanche-transistor generator is controlled by an open-circuited delay line; (*b*) an equivalent circuit after the transistor is triggered; (*c*) the reflection chart for the line current.

The output voltage step is negative and has a maximum magnitude of $V/2$ because $R_L \leq R_o$.

The pulse which appears across R_L in Fig. 13-28*b* results from the differentiation of the step generated by the avalanche transistor by the R_LC differentiating circuit. On this basis we may see that, in going from the circuit of Fig. 13-28*b* to the circuit of Fig. 13-30, we have replaced the R_LC differentiation by delay-line differentiation, as described in Sec. 3-16.

We have assumed that the circuits of Figs. 13-28*b* and 13-30*a* were externally triggered. Either circuit may be rendered astable by raising V_{CC} or returning R_b to a bias voltage such that avalanche breakdown occurs without the need for an external trigger.

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